"Rule synchronization" in P systems

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The idea of rule synchronization

$$\begin{bmatrix} a^n b^m u \\ b \to bd \otimes au \to u \end{bmatrix}$$

Fig. 1. Multiplication by using synchronization

[Bogdan Aman, Gabriel Ciobanu: Synchronization of Rules in Membrane Computing. In: *Proc. CMC 20*, 257-268.]



$$a^{n}b^{m}u$$

$$b \rightarrow bd \otimes au \rightarrow u$$

$$a^{n}5^{m}u$$

$$a^{n-1}(bd)^{m}u$$

$$a^{n-2}(bd^{2})^{m}u$$

$$(bd^{n})^{m}u$$

$$(bd^{n})^{m}u$$

$$(bd^{n})^{m}u$$

$$(bd^{n})^{m}u$$

$$(bd^{n})^{m}u$$



Notice:





Convenient way to simulate register machines

- The value of register r corresponds to the multiplicity of a_r
- Labels I_i govern the functioning

 $l_1: (ADD(r), l_2, l_3),$



Fig. 3. Simulating ADD instruction.



[Bogdan Aman, Gabriel Ciobanu: Synchronization of Rules in Membrane Computing. In: *Proc. CMC 20*, 257-268.]

Convenient way to simulate register machines

$$\begin{split} l_{1} : (SUB(r), l_{2}, l_{3}) \\ r_{21} : l_{1} \to l_{1}', \\ r_{22} : a_{r}u \to v, \\ r_{23} : l_{1}' \to l_{2}, \\ r_{24} : v \to u, \\ r_{25} : l_{1}' \to l_{3}u, \\ r_{26} : u \to \varepsilon, \end{split}$$





Fig. 4. Simulating SUB instruction.

Our first question

- Rule synchronization and maximal parallelism can simulate Turing machines
- Without rule synchronization we also get the maximal Turing machine equivalent power

• What happens if we have rule synchronization without the maximal parallelism – with "free" rule application?



Our answer

- Petri nets can be viewed as computing models
- Simple place-transition are **less powerful** than Turing machines

 Rule synchronized systems with free rule application can be simulated by simple place-transition nets





Fig. 1. Assume that $w_1^0 = a^3 b^3 c^2$, $w_2^0 = d$ and $r = ab^2 c^2 \rightarrow ac^3 (d, in_2)^3$. The figure on the left shows the arcs pointing to transition t_r together with their weights, the figure on the right shows the arcs going out from transition t_r together with their weights.





Our second question/research suggestion

- With rule synchronization we can "do **arithmetic**" conveniently
- Can we use this to convert ordinary P systems to reversible systems?



Why is reversibility interesting?

Landauer's principle – **theoretical lower bound** on the energy consumption of computation

- The logically irreversible operations necessarily dissipate energy
- Landauer limit: the **minimum possible amount** of energy required to **erase one bit** of information is

*k·T·*ln *2*

where k is the Boltzmann constant, T is the temperature of the circuit in Kelvins



The idea

- If the number of possible different transitions is bounded,
- we can record the "computation history" inside the system, and
- use this history to make the machine "backwards deterministic".



[Charles H. Bennett, Logical reversibility of computation. *IBM journal of Research and Development* 17.6 (1973): 525-532.]

Stage	Quadruples	Contents of tape		
		Working tape	History tape	Output tape
		INPUT		
	1) $\begin{cases} A_1[b \mid b] \to [b+b]A_1' \\ A_1'[b \mid] \to [+1 \ 0]A_2 \end{cases}$			
Compute ^a	$m) \qquad \begin{cases} A_{j}[T \mid b] \rightarrow [T' + b]A_{m}' \\ A_{m}'[/b \mid] \rightarrow [\sigma m \ 0]A_{k} \end{cases}$			
	$N) \begin{cases} A_{f-1}[b \mid b] \rightarrow [b+b]A_{N}' \\ A'[l \mid b \mid] \rightarrow [0 \mid N \mid 0]A_{N} \end{cases}$			
	$(M_N [107]) \times [0000]M_f$	OUTPUT	HISTORY	
Copy output ^b	$A_{f}[b \ N \ b] \rightarrow [b \ N \ b]B_{1}'$	—	_	_
	$B_1'[//] \rightarrow [+0+]B_1$			
	$x \neq b: \{ B_1[x \ N \ b] \rightarrow [x \ N \ x]B_1' \}$			
	$B_{1}[b \ N \ b] \rightarrow [b \ N \ b]B_{2}'$			
	$B_2'[//] \rightarrow [-0]B_2$			
	$x \neq b$: { $B_2[x N x] \rightarrow [x N x]B_2'$ }			
	$B_2[b \ N \ b] \to [b \ N \ b]C_f$	<u> </u>		61 ITD1 II
Retrace		_OUTPUT	HISTORY	
	$N) \qquad \begin{cases} C_{f}[fN] \rightarrow [0 \ b \ 0]C_{N} \\ C_{N}'[b \ b] \rightarrow [b - b]C_{f-1} \end{cases}$			
	$m) \qquad \begin{cases} C_k[/m/] \rightarrow [-\sigma \ b \ 0]C_m' \\ C_m'[T'/b] \rightarrow [T-b]C_j \end{cases}$			
	1) $\begin{cases} C_2[/1/] \rightarrow [-b\ 0]C_1' \\ C_2[/h] \rightarrow [h-h]C \end{cases}$			
	$(C_1[0, 0]) \rightarrow [0, 0]C_1$	INPUT		OUTPU

The idea



The arithmetic we need





Division

 $a^{n}b^{m}u_{1}$ $b \rightarrow bd \otimes u_{1} \rightarrow u_{2}$ $ab \rightarrow \varepsilon \otimes u_{2} \rightarrow u_{3}u_{0} \otimes d \rightarrow r$ $u_{0} \rightarrow u_{0}' \quad au_{3} \rightarrow au_{3a} \quad bu_{3} \rightarrow bu_{3b}$ $u_{3a} \rightarrow u_{1}c \otimes r \rightarrow b \otimes u_{0}' \rightarrow \varepsilon$ $u_{3b} \rightarrow \varepsilon \otimes br \rightarrow \varepsilon \otimes u_{0}' \rightarrow \varepsilon$ $u_{3} \rightarrow c \otimes r \rightarrow \varepsilon \otimes u_{0}' \rightarrow \varepsilon$



Fig. 2. Division by using synchronization



[Bogdan Aman, Gabriel Ciobanu: Synchronization of Rules in Membrane Computing. In: *Proc. CMC 20*, 257-268.]

How can rule synchronization be useful?





A problem

- What do we mean by "transition 2"?
- Do the **rule combinations** identify the **transitions** in a way that is necessary?



No. A simple example



 $aaaaa => aaaaaaaaa<math>a^5 => a^8$ $aaaaa => aaaaaaa<math>a^5 => a^6$

aaaaa => aaaaaa $a^5 => a^6$ aaaa => aaaaaa $a^4 => a^6$



Related question

- How to **avoid "ambiguous**" situations?
- Avoid maximal **parallelism** let **all rules** in the rule "tuple" be executed **exactly once**?
- Are there **special cases** where maximal **parallel application** makes **no trouble**?
- What is the **power of** these possibly "**reversible**" variants?



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